Amendments to the Specification:

Please replace the paragraph beginning at page 17, line 14, with the following rewritten paragraph:

Then, when reading out data of memory capacitor 15, each voltage of the word lines 13 for memory, the word lines 14 for reference, the plate lines 17 for memory, and plate lines 18 for reference is controlled in the timing shown in Fig. 7. Accordingly, the voltage of the bit lines for memory 19 and the bit lines for reference 20 varies based on the data of the memory capacitor 15. The voltage is controlled by the plate driver 22 and the row ~~driver 23~~ decoder 21 .